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Appendix

Marked Up Copy of Specification showing changes

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LOW JITTER INPUT BUFFER WITH SMALL INPUT SIGNAL SWING

Background of the Invention

Field of the Invention

5   [0001] The present invention generally relates to an interface circuit, and

particularly to a low jitter input buffer.

Description of Related Art

[0002]   Major design efforts have been directed at circuit design techniques

involving input circuits for memory devices. A number of solutions have

10   been proposed.

[0003]   U.S. Patent 5,978,310 (Bae et al) describes an input buffer for a

DRAM memory device, which removes noise from the row address strobe.

The device has a data output enable, which can be delayed for a

predetermined time, and which also produces a contr o! signal for the

15   output. There is also a buffer output for producing the noise free input

according to the control signal.

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[0004]   U.S. Patent 6,002,618 (Komarek et al) discloses an NMOS input receiver circuit for a read only memory. It includes a feedback loop to control hysteresis. There is a second stage and an additional output for the receiver. Switching noise from inside the memory is isolated and cannot be fed back into the receiver circuit to affect the TTL voltage levels. Wide, long FET sizes are used to minimize manufacture variations in the receiver switching levels.

[0005]   What is still needed is a mechanism by which an input buffer works in the presence of ground noise, specifically how capacitance can be used to reduce such noise for a memory input circuit.

Summary of the Invention

[0006]   It is therefore an object of the present invention to provide an efficient circuit design technique for an input buffer receiver for a particular memory device[[,]] that works to filter ground noise. It is a further object of the invention to provide a means for reducing jitter in an input buffer. This is achieved by attaching a large capacitance to the ~~PMOS~~ bias node of the input buffer receiver.

[0007]   These and other objects are achieved by an input buffer receiver comprising: a buffer input portion for receiving an input signal ~~SIGNAL_IN~~;

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a large ~~capacitor~~ capacitance ~~CHC~~ between a ~~PMOS~~ bias node and a ~~VSS source~~ lower supply voltage VSS, and a buffer output portion for producing an output signal ~~SIGNAL_OUT1~~. Furthermore, in the input buffer receiver, the ~~VB11 gate~~ biasing voltage of the bias node ~~of transistors P11 and P12~~ is charge coupled to the ~~VSS~~ lower voltage source ~~voltage~~. This results in a quicker response time for the output signal ~~SIGNAL_OUT1~~.

Brief Description of the Drawings

[0008]   The foregoing and other objects, aspects, and advantages will be better understood from the following detailed description of a preferred embodiment of the invention, with reference to the drawings, in which:

[0009]   FIG. 1 is a diagram of an input buffer receiver according to the prior art.

[0010]   FIG. 2 is a diagram of an input buffer receiver according to the present invention.

[0011]   FIGS.3A-B show the timing diagrams of the input buffer receiver of the present invention and the definitions of JITTER_RISE and JITTER_FALL.

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[0012]   FIGS. 4A-B illustrate the workings of ~~capacitance~~ _capacitor_ CHC to reduce JITTER_RISE and JITTER_FALL.

Detailed Description of the Invention

[0013]   One embodiment of the present invention is provided below with reference to the accompanying diagrams.

[0014]   Referring to FIG. 1, the input buffer receiver of the prior art includes a buffer input portion 100 for receiving an input signal SIGNAL_IN and a buffer output portion 200 for producing an output signal SIGNAL_OUT.

[0015]   The buffer input portion 100 is comprised of: NMOS transistors N1 and N2, where a lower supply voltage VSS is applied to the source nodes of NMOS transistors N1 and N2, and PMOS transistors P1 and P2, where an upper voltage supply VDD is applied to the source nodes. _The gate nodes of transistors P1 and P2 and the the drains of transistors N1 and P1 are connected together to form the biasing node b1. The biasing voltage VB1 is developed at the biasing node b1 as a result of the configuration of transistors P1 and P2. A parasitic capacitor Cp is present from the biasing node b1 to the ground reference node._ ~~and a signal VB1 is applied to the gate nodes of P1 and P2.~~ In the prior art, a reference voltage VREF is applied to the gate of _transistor_ N1, _input signal_ SIGNAL_IN is applied to

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the gate of <u>transistor</u> N2, ~~and VB1 is applied to the drain of N1 and the~~

~~drain of P1, as well as the PMOS bias node of P1 and P2~~. <u>Input signal</u>

SIGNAL_IN is a low swing signal coming from off chip. The buffer output

portion 200 is comprised of a common node for the drain of <u>transistor</u> N2

and drain of <u>transistor</u> P2, which serves as input to inverter I1. The output

of inverter I1 is the output signal <u>output</u> SIGNAL_OUT.

[0016]   <u>The ground noise (VSS noise), as described above, is developed</u>

<u>between the lower supply voltage VSS and the ground reference voltage.</u>

<u>The magnitude of the VSS noise affects the delay timing from the input</u>

<u>signal SIGNAL_IN to the output signal SIGNAL_OUT. The variation in the</u>

<u>delay causes jitter in the rise and fall delays of the buffer and thus slower</u>

<u>response times.</u>

[0017]   Referring to FIG. 2, the proposed invention is comprised of a similar

buffer input portion 101 and a similar buffer output portion 201. The buffer

input portion 101 is comprised of: NMOS transistors N11 and N12, where

~~a~~ <u>the</u> lower supply voltage VSS is applied to the source nodes of N11 and

N12, and PMOS transistors P11 and P12, where an upper supply voltage

VDD is applied to the source nodes. <u>The gate nodes of transistors P11</u>

<u>and P12 and the the drains of transistors N11 and P11 are connected</u>

<u>together to form the biasing node b11. The biasing voltage VB11 is</u>

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developed at the biasing node b11 as a result of the configuration of transistors P11 and P12. A parasitic capacitor Cp is present from the biasing node b11 to the ground reference node. ~~A signal VB11 is applied to the gate nodes of P11 and P12.~~ A reference supply voltage VREF is applied to the gate of transistor N11, input signal SIGNAL_IN is applied to the gate of N12~~, and VB11 is applied to the drain of N11 and the drain of P11~~. In the present invention, a large ~~capacitance~~ capacitor CHC is attached between the ~~PMOS~~ bias node ~~VB11~~ b11 and the lower supply ~~source~~ voltage VSS. The buffer output portion 201 is comprised of a common node for the drain of transistor N12 and the drain of transistor P12, which serves as input to inverter I11. The output of inverter I11 is the output signal SIGNAL_OUT1 of the invention.

[0018]   The large capacitance CHC is in series with the parasitic capacitor Cp ~~capacitance~~ of the input buffer receiver ~~devices~~ transistors N11, P11, and P12. The large capacitor CHC, as connected, is designed to have an extremely large capacitance relative to the parasitic capacitor Cp such that the bias voltage VB11 essentially follows the voltage changes in the lower supply voltage VSS preventing the effects of the VSS noise. This coupling ratio is determined by the formula:

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$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor CHC.

Cp is the capacitance value of the parasitic capacitor Cp.

[0019]   Because of its large coupling ratio (very close to 1), the capacitor CHC essentially charge couples the biasing voltage VB11 gate voltage of the PMOS bias node b11, to the VSS source lower supply voltage VSS, of devices N11 and N12. This forces the transistors N11 and N12 to activate and deactivate essentially simultaneously, allowing for a quicker response time on output signal SIGNAL_OUT1.

[0020]   FIGS. 3A-B are diagrams of timed operation showing the input signal SIGNAL_IN, the source lower supply voltage VSS, and the output signal SIGNAL_OUT1 of the proposed invention. It should be noted that the input signal SIGNAL_IN is defined as VIH=VREF+350mv and VIL=VREF-350mv, and VSS is 200mv. The output signal SIGNAL_OUT1 is defined by the delayed signal delay times DELTA1 or DELTA2, when

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input signal SIGNAL_IN rises, and the delay times DELTA3 or DELTA4,

when the input signal SIGNAL_IN falls. The delay time DELTA1 is defined

as the delay from the rising edge of input signal SIGNAL_IN to the rising

edge of output signal SIGNAL_OUT, when VSS=200mv. It is the delay on

output signal SIGNAL_OUT1 when transistor N12 sees VSS noise and

turns on weakly. The delay time DELTA2 is defined as the delay from the

rising edge of input signal SIGNAL_IN to the rising edge of output signal

SIGNAL_OUT1, when VSS=0v. It is the delay on of the output signal

SIGNAL_OUT1 when transistor N12 does not see VSS noise and turns on

strongly. The delay time DELTA3 is defined as the delay from the falling

edge of input signal SIGNAL_IN to the falling edge of output

SIGNAL_OUT1, when VSS=0v. It is the delay on of the input signal

SIGNAL_OUT1 when transistor N12 does not see VSS noise and turns off

weakly. DELTA4 is defined as the delay from the falling edge of input

signal SIGNAL_IN to the falling edge of output signal SIGNAL_OUT1,

when VSS=200mv. It is the delay seen on output signal SIGNAL_OUT1

when transistor N12 sees VSS noise and turns off strongly. By definition,

the delay times DELTA2 and DELTA4 are smaller than the delay times

DELTA1 and DELTA3. The rise time jitter JITTER_RISE is the difference

between the delay times DELTA1 and DELTA2 when the input signal

SIGNAL_IN rises and the fall time jitter JITTER_FALL is the difference

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between the delay times DELTA3 and DELTA4 when input signal

SIGNAL_IN falls. The intent of the invention ~~capacitance~~ large capacitor

CHC is to reduce rise time jitter JITTER_RISE and fall time jitter

JITTER_FALL by primarily having ~~devices~~ transistors P12 and N12,

activate, in the presence or absence of ground noise, almost

simultaneously.

[0021]   FIGS. 4A-B illustrate the workings of large capacitor CHC. In Fig.

4a, the large capacitor is shown in series with the parasitic capacitor Cp.

The ~~Its~~ large capacitance coupling ratio of the large capacitor CHC versus

the capacitance of the parasitic capacitor Cp creates a charge coupling

~~couples~~ of the ~~PMOS~~ bias node, ~~VB11~~ b11, of the input buffer receiver, to

the ~~VSS source~~ lower supply voltage VSS, of the input buffer receiver.

This results in a quicker response time for a input signal SIGNAL_OUT1.

[0022]   While the invention has been described in terms of the preferred

embodiments, those skilled in the art will recognize that various changes

in form and details may be made without departing from the spirit and

scope of the invention. The present invention covers modifications that fall

within the range of the appended claims and their equivalents.

[0023]   While this invention has been particularly shown and described with

reference to the preferred embodiments thereof, it will be understood by

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those skilled in the art that various changes in form and details may be

made without departing from the spirit and scope of the invention.

[0024]   What is claimed is:

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1. (Currently Amended) An input buffer receiver comprising:

    a buffer input portion for receiving an input signal SIGNAL_IN, said

    buffer input portion comprising a bias node;

    a large capacitor capacitance between a PMOS the bias node and

    a VSS source lower supply voltage said large capacitor

    providing a coupling ratio between said large capacitor and a

    parasitic capacitor coupled between said bias node and a

    ground reference point approaching a unity value such that a

    biasing voltage at said biasing node follows said lower supply

    voltage to minimize effects of a ground noise signal between the

    lower supply voltage and the ground reference point; and

    a buffer output portion in communication with the buffer input

    portion for producing an output signal SIGNAL_OUT1.

2. (Currently Amended) The input buffer receiver of claim 1, wherein the

    buffer input portion which receives an the input signal SIGNAL_IN further

    comprises:

    a first transistor of a first conductivity type N11 having a source

    node to which a VSS source the lower supply voltage is applied,

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6   a gate node to which a reference voltage ~~VREF~~ is applied, and

7   a drain node <u>at which the biasing voltage is developed</u> ~~to which~~

8   ~~a signal VB11 is applied~~;

9   a second transistor <u>of a second conductivity type</u> ~~P11~~ having a

10   drain node which is connected to the drain node of the first

11   transistor ~~N11~~, and a gate node <u>at which the biasing voltage is</u>

12   <u>developed</u> ~~to which a signal VB11 is applied~~, and a source node

13   to which an upper supply voltage <u>source</u> ~~VDD~~ is applied;

14   a third transistor <u>of the second conductivity type</u> ~~P12~~ having a drain

15   node which is connected to the drain of a fourth transistor ~~N12~~,

16   a gate node <u>at which the biasing voltage is developed</u> ~~to which~~

17   ~~a signal VB11 is applied~~, and a source node to which ~~an~~ <u>the</u>

18   upper supply voltage <u>source</u> ~~VDD~~ is applied;

19   a fourth transistor <u>of the first conductivity type</u> ~~N12~~ having a source

20   node to which ~~a VSS source~~ <u>lower suppply</u> voltage is applied, a

21   gate node to which an input signal ~~SIGNAL_IN~~ is applied

22   externally, and a drain node which is ~~the~~ <u>an</u> input to the buffer

23   output portion.

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3. (Currently Amended) The input buffer receiver of claim 2~~1~~, wherein the first and fourth transistors, ~~N11 and N12,~~ are NMOS transistors, and the second and third transistors, ~~P11 and P12,~~ are PMOS transistors.

4. (Currently Amended) The input buffer receiver of claim 2~~1~~, wherein the large capacitor ~~capacitance~~ is connected between the sources of the first and fourth transistors, ~~N11 and N12,~~ of the buffer input portion and the gate of the second transistor ~~P11~~ of the buffer input portion.

5. (Currently Amended) The input buffer receiver of claim 2~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to its drain.

6. (Currently Amended) The input buffer receiver of claim 2~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to the drain of the first transistor ~~N11~~.

7. (Currently Amended) The input buffer receiver of claim 2~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to the gate of the third transistor ~~P12~~.

8. (Currently Amended) The input buffer receiver of claim 2~~1~~, wherein the buffer output portion which produces ~~an~~ output signal ~~SIGNAL_OUT1~~

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3 comprises: a first inverter I11 connected to the drain of the third transistor

4 P12 and the drain of the fourth transistor N12;

1 9. (Currently Amended) The input buffer receiver of claim 2 1, wherein P12

2 and N12 the third transistor and the fourth transistor activate almost

3 simultaneously to provide an efficient circuit design technique for filtering

4 minimize the effects of ground noise on a delay jitter factor of said input

5 buffer.

1 10. (Currently Amended) The input buffer receiver of claim 1, involving a large

2 capacitance coupling ratio, which wherein the large capacitor charge

3 couples the PMOS bias node of the input buffer receiver to the VSS

4 source lower supply voltage of the input buffer receiver and wherein a

5 capacitance value of the large capacitor is selected by the formula:

6 $$\frac{CHC}{Cp + CHC} \approx 1$$

7 where:

8 CHC is the capacitance value of the large capacitor,

9 and

10 Cp is the capacitance value of the parasitic capacitor.

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11. (Currently Amended) The input buffer receiver of claim 1, ~~involving a~~ wherein the capacitance value of the large capacitor relative to said parasitic capacitor ~~capacitance coupling ratio, which~~ results in a quicker response time for the output signal ~~a SIGNAL_OUT1~~.

12. (New) An integrated circuit formed on a substrate comprising:

an input buffer receiver for receiving an input signal and connected to said distribution network, said input buffer comprising:

a buffer input portion for receiving the input signal, said buffer input portion comprising a bias node;

a large capacitor between the bias node and a lower supply voltage, said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point ; and

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15   a buffer output portion in communication with the buffer

16   input portion for producing an output signal.

1   13.   (New) The integrated circuit of claim 12, wherein the buffer input portion of

2   the input buffer receiver further comprises:

3   a first transistor of a first conductivity type having a source node to

4   which the lower supply voltage is applied, a gate node to which

5   a reference voltage is applied, and a drain node at which the

6   biasing voltage is developed ;

7   a second transistor of a second conductivity type having a drain

8   node which is connected to the drain node of the first transistor,

9   and a gate node at which the biasing voltage is developed, and

10   a source node to which an upper supply voltage source is

11   applied;

12   a third transistor of the second conductivity type having a drain

13   node which is connected to the drain of a fourth transistor, a

14   gate node at which the biasing voltage is developed, and a

15   source node to which the upper supply voltage source is

16   applied;

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17   a fourth transistor of the first conductivity type having a source node

18   to which lower supply voltage is applied, a gate node to which

19   an input signal is applied externally, and a drain node which is

20   an input to the buffer output portion.

1   14.   (New) The integrated circuit of claim 13, wherein the first and fourth

2   transistors are NMOS transistors, and the second and third transistors are

3   PMOS transistors.

1   15.   (New) The integrated circuit of claim 13, wherein the large capacitor is

2   connected between the sources of the first and fourth transistorsof the

3   buffer input portion and the gate of the second transistor of the buffer input

4   portion.

1   16.   (New) The integrated circuit of claim 13, wherein the gate of the second

2   transistor is connected to its drain.

1   17.   (New) The integrated circuit of claim 13, wherein the gate of the second

2   transistor is connected to the drain of the first transistor.

1   18.   (New) The integrated circuit of claim 13, wherein the gate of the second

2   transistor is connected to the gate of the third transistor.

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1   19.   (New) The integrated circuit of claim 13, wherein the buffer output portion

2   which produces output signal comprises: a first inverter connected to the

3   drain of the third transistor and the drain of the fourth transistor;

1   20.   (New) The integrated circuit of claim 13, wherein the third transistor and

2   the fourth transistor activate almost simultaneously to minimize the effects

3   of ground noise on a delay jitter factor of said input buffer.

1   21.   (New) The integrated circuit of claim 12, wherein the large capacitor

2   charge couples the bias node of the input buffer receiver to the lower

3   supply voltage of the input buffer receiver and wherein a capacitance

4   value of the large capacitor is selected by the formula:

5
$$\frac{CHC}{Cp + CHC} \approx 1$$

6   where:

7   **CHC** is the capacitance value of the large capacitor,

8   and

9   **Cp** is the capacitance value of the parasitic capacitor.

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1   22.   (New) The integrated circuit of claim 12, wherein the capacitance value of

2   the large capacitor relative to said parasitic capacitor results in a quicker

3   response time for the output signal.

1   23.   (New) A method for minimizing effects of ground noise on an input buffer

2   receiver comprising the steps of:

3   forming a buffer input portion for receiving an input signal on a

4   substrate;

5   forming a bias node within said buffer input portion;

6   connecting said a lower supply voltage to said buffer input portion;

7   forming a large capacitor between the bias node and the lower

8   supply voltage said large capacitor providing a coupling ratio

9   between said large capacitor and a parasitic capacitor coupled

10   between said bias node and a ground reference point

11   approaching a unity value such that a biasing voltage at said

12   biasing node follows said lower supply voltage to minimize

13   effects of a ground noise signal between the lower supply

14   voltage and the ground reference point; and

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15   forming a buffer output portion on said substrate in communication

16   with the buffer input portion for producing an output signal.

1   24.   (New) The method of claim 23, wherein forming the buffer input portion

2   further comprises the steps of:

3   forming a first transistor of a first conductivity type on said

4   substrate;

5   applying the lower supply voltage to a source node of the first

6   transistor;

7   applying a reference voltage to a gate node of the first transistor;

8   connecting a drain node of the first transistor to develop as biasing

9   voltage at said drain node;

10   forming a second transistor of a second conductivity type on said

11   substrate;

12   connecting a drain node of the second transistor to the drain node

13   of the first transistor;

14   connecting a gate node of the second transistor to the drain node of

15   the first transistor for developing the biasing voltage; and

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16   connecting a source node of the second transistor to an upper

17   supply voltage;

18   forming a third transistor of the second conductivity type on said

19   substrate;

20   connecting a drain node of the third transistor to the drain of a

21   fourth transistor;

22   connecting a gate node of the third transistor to the drain node of

23   the first transistor for developing the biasing voltage;

24   connecting a source node of the third transistor to the upper supply

25   voltage source;

26   forming a fourth transistor of the first conductivity type on said

27   substrate;

28   connecting a source node of the fourth transistor to the lower

29   supply voltage;

30   connecting a gate node of the fourth transistor to receive an input

31   signal externally; and

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32   connecting a drain node of the fourth transistor to an input to the

33   buffer output portion.

1   25.   (New) The method of claim 24, wherein the first and fourth transistors are

2   NMOS transistors, and the second and third transistors are PMOS

3   transistors.

1   26.   (New) The method of claim 24, wherein forming the large capacitor

2   comprises the step of:

3   connecting said large capacitor between the sources of the first and

4   fourth transistors of the buffer input portion and the gate of the

5   second transistor of the buffer input portion.

1   27.   (New) The method of claim 24, wherein forming the buffer input portion

2   further comprises the steps of:

3   connecting the gate of the second transistor to its drain.

1   28.   (New) The method of claim 24, wherein forming the buffer input portion

2   further comprises the steps of:

3   connecting the gate of the second transistor to the gate of the third

4   transistor.

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1   29.   (New) The method of claim 24, wherein forming the buffer output portion

2   which produces output signal comprises the step of:

3   forming a first inverter on said substrate; and

4   connecting an input of said first inverter to the drain of the third

5   transistor and the drain of the fourth transistor;

1   30.   (New) The method of claim 24, wherein the third transistor and the fourth

2   transistor activate almost simultaneously to minimize the effects of ground

3   noise on a delay jitter factor of said input buffer.

1   31.   (New) The method of claim 23, wherein the large capacitor charge

2   couples the bias node of the input buffer receiver to the lower supply

3   voltage of the input buffer receiver and wherein a capacitance value of the

4   large capacitor is selected by the formula:

5
$$\frac{CHC}{Cp + CHC} \approx 1$$

6   where:

7   CHC is the capacitance value of the large capacitor,

8   and

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9   **Cp** is the capacitance value of the parasitic capacitor.

1   32.   (New) The method of claim 23, wherein the capacitance value of the large

2   capacitor relative to said parasitic capacitor results in a quicker response

3   time for the output signal.

1   33.   (New) An apparatus for minimizing effects of ground noise on an input

2   buffer receiver comprising:

3   means for forming a buffer input portion for receiving an input signal

4   on a substrate;

5   means for forming a bias node within said buffer input portion;

6   means for connecting said a lower supply voltage to said buffer

7   input portion;

8   means for forming a large capacitor between the bias node and the

9   lower supply voltage said large capacitor providing a coupling

10   ratio between said large capacitor and a parasitic capacitor

11   coupled between said bias node and a ground reference point

12   approaching a unity value such that a biasing voltage at said

13   biasing node follows said lower supply voltage to minimize

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14   effects of a ground noise signal between the lower supply

15   voltage and the ground reference point; and

16   means for forming a buffer output portion on said substrate in

17   communication with the buffer input portion for producing an

18   output signal.

1   34.   (New) The apparatus of claim 23, wherein forming the buffer input portion

2   further comprises:

3   means for forming a first transistor of a first conductivity type on

4   said substrate;

5   means for applying the lower supply voltage to a source node of the

6   first transistor;

7   means for applying a reference voltage to a gate node of the first

8   transistor;

9   means for connecting a drain node of the first transistor to develop

10   as biasing voltage at said drain node;

11   means for forming a second transistor of a second conductivity type

12   on said substrate;

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13   means for connecting a drain node of the second transistor to the

14   drain node of the first transistor;

15   means for connecting a gate node of the second transistor to the

16   drain node of the first transistor for developing the biasing

17   voltage; and

18   means for connecting a source node of the second transistor to an

19   upper supply voltage;

20   means for forming a third transistor of the second conductivity type

21   on said substrate;

22   means for connecting a drain node of the third transistor to the

23   drain of a fourth transistor;

24   means for connecting a gate node of the third transistor to the drain

25   node of the first transistor for developing the biasing voltage;

26   means for connecting a source node of the third transistor to the

27   upper supply voltage source;

28   means for forming a fourth transistor of the first conductivity type on

29   said substrate;

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30   means for connecting a source node of the fourth transistor to the

31   lower supply voltage;

32   means for connecting a gate node of the fourth transistor to receive

33   an input signal externally; and

34   connecting a drain node of the fourth transistor to an input to the

35   buffer output portion.

1   35.   (New) The apparatus of claim 24, wherein the first and fourth transistors

2   are NMOS transistors, and the second and third transistors are PMOS

3   transistors.

1   36.   (New) The apparatus of claim 24, wherein means for forming the large

2   capacitor comprises:

3   means for connecting said large capacitor between the sources of

4   the first and fourth transistors of the buffer input portion and the

5   gate of the second transistor of the buffer input portion.

1   37.   (New) The apparatus of claim 24, wherein means for forming the buffer

2   input portion further comprises:

3   means for connecting the gate of the second transistor to its drain.

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1 38. (New) The apparatus of claim 24, wherein means for forming the buffer

2   input portion further comprises the steps of:

3   means for connecting the gate of the second transistor to the gate

4   of the third transistor.

1 39. (New) The apparatus of claim 24, wherein means for forming the buffer

2   output portion which produces output signal comprises:

3   means for forming a first inverter on said substrate; and

4   means for connecting an input of said first inverter to the drain of

5   the third transistor and the drain of the fourth transistor;

1 40. (New) The apparatus of claim 24, wherein the third transistor and the

2   fourth transistor activate almost simultaneously to minimize the effects of

3   ground noise on a delay jitter factor of said input buffer.

1 41. (New) The apparatus of claim 23, wherein the large capacitor charge

2   couples the bias node of the input buffer receiver to the lower supply

3   voltage of the input buffer receiver and wherein a capacitance value of the

4   large capacitor is selected by the formula:

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$$\frac{CHC}{Cp + CHC} \approx 1$$

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6   where:

7   **CHC** is the capacitance value of the large capacitor

8   CHC, and

9   **Cp** is the capacitance value of the parasitic capacitor

10   Cp.

1   42.   (New) The apparatus of claim 23, wherein the capacitance value of the

2   large capacitor relative to said parasitic capacitor results in a quicker

3   response time for the output signal.

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Abstract

[0025]   A particular input buffer receiver includes a buffer input portion for

receiving an input signal SIGNAL_IN, a large capacitor capacitance CHC

between the PMOS a bias node and the VSS source lower supply voltage,

and a buffer output portion for producing an output signal SIGNAL_OUT1.

The circuit works to remove ground noise by charge coupling the VB11

bias voltage developed at the bias node to the VSS source lower supply

voltage of the input device.

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